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RM-7141

B. E. III (Sem. VI) (I. T.) Examination

May / June – 2010

Computer Architecture & Peripherals

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 3 (Sem. 6) (I. T.)**

Name of the Subject :

☛ **Computer Architecture & Peripherals**

☛ Subject Code No. : **7 1 4 1** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Answer the two sections in separate answer books.
(3) Figures to extreme right indicate maximum marks.
(4) Make necessary assumptions and clearly mention them, if required.
(5) Support your answers with block diagram or neat sketches, if required.

SECTION - I

1 (a) Answer the following qeustions : **10**

(1) State the use of FGI and FGO. **2**

(2) How many references are needed for direct and indirect instruction to bring an operand into processor register ? **1**

(3) Define following : **4**

(i) Special bit
(ii) Effective address
(iii) Microinstruction
(iv) Throughput.

(4) Write full form of the following : **2**

(i) PSW
(ii) MIMD.

(5) What is delayed load ? **1**

(b) Answer the following questions : **10**

(i) Explain in brief major difficulties that cause instruction pipeline to deviate from its normal operation.

(ii) The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is. 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F : **6**

(a) What is the instruction that will be fatched and executed next ?

(b) Show the binary operation that will be performed in the AC. When the instruction is executed.

(c) Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and the sequence counter SC in binary at the end of the instruction cycle.

2 (a) Write difference between RISC and CISC. **5**

(b) (1) Draw and explain flowchart of instruction cycle with interrupt. **8**

(2) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline. **2**

OR

(b) (1) Write a program to evaluate the following arithmetic statement. **4**

X=(A+B)* (C+D)

(a) Using a general register computer with three address instructions.

(b) Using a stack organized computer with zero-address operation instruction.

(2) Explain Microprogram sequencer for a control memory. **6**

3 (a) For what purpose conputer uses concept of addressng mode ? Explain any five addressing modes. **8**

(b) What is pipeline ? Explain RISC pipeline. **7**

OR

(b) Explain Input-Output configuration. **7**

SECTION - II

4 (a) Define the following terms : **10**

(1) Locality of reference

(2) Loosely coupled multiprocessor

(3) Auxiliary Memory

(4) Interrupt vector

(5) Page Falut.

(b) Attempt the following questions :

(1) Explain CPU-IOP communication. **5**

(2) Explain Content Addressable memory. **5**

5 (a) Explain Asynchronous data transfer with destination initiated transfer using handshaking mechanism. **8**

(b) What is the use of TLB in virtual memory system ? **2**

OR

5 (a) Explain algorithm for addition and subtraction of floating point numbers with flowchart. **8**

(b) A computer system has a cache and main memory. If a referenced word is in the cache and 20 ns are required to access it. Main memory access time is 200 ns. Calculate average memory access time when a hit ratio is 0.9. **2**

(c) Explain 4×4 FIFO buffer using circuit diagram. **5**

6 Attempt the following questions : (any **three**) **15**

(1) Draw the flowchart for decimal multiplication and decimal division operation.

(2) Explain source-initiated Handshaking for Asynchronous data transfer.

(3) Compare and constrat between memory space and address space.

(4) Explain DMA controller.

(5) What is mutual exclusion ? Explain mutual exclusion with semaphore.